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Papers will include discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors,

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and universities.

This book introduces readers to the most advanced research results on Design for Manufacturability (DFM) with multiple patterning lithography (MPL) and electron beam lithography (EBL). The authors describe in detail a set of algorithms/methodologies to resolve issues in modern design for manufacturability problems with advanced lithography. Unlike books that discuss DFM from the product level or physical manufacturing level, this book describes DFM solutions from a circuit design level, such that most of the

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critical problems can be formulated and solved through combinatorial algorithms.

This book proposes a synergistic framework to help IP vendors to protect hardware IP privacy and integrity from design, optimization, and evaluation perspectives. The proposed framework consists of five interacting components that directly target at the primary IP violations. All the five algorithms are developed based on rigorous mathematical modeling for primary IP violations and focus on different stages of IC design, which can be

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combined to provide a formal security guarantee.

This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.

An examination of how, in practice, the effective verification of various arms control treaties - including a comprehensive test ban

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treaty, conventional forces reductions, a fissile material cut-off and a freeze on the development and production of nuclear weapons - can be achieved.

This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the

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field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation,

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Hardware/Software Co-  
verification, Power  
Performance Area (PPA)  
analysis on a virtual  
platform, Reuse Methodology  
from Algorithm/ESL to RTL,  
and other overall  
methodologies.

This book constitutes the  
refereed proceedings of the  
9th International IFIP WG  
2.13 Conference on Open  
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held in Koper-Capodistria,  
Slovenia, in June 2013. The  
18 revised full papers and 3  
short papers presented were  
carefully reviewed and  
selected. The papers are  
organized in topical  
sections on innovation and

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sustainability; practices and methods; FOSS technologies; security and open standards; and business models and licensing.

This book introduces readers to a variety of tools for automatic analog integrated circuit (IC) sizing and optimization. The authors provide a historical perspective on the early methods proposed to tackle automatic analog circuit sizing, with emphasis on the methodologies to size and optimize the circuit, and on the methodologies to estimate the circuit's performance. The discussion also includes robust circuit

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design and optimization and the most recent advances in layout-aware analog sizing approaches. The authors describe a methodology for an automatic flow for analog IC design, including details of the inputs and interfaces, multi-objective optimization techniques, and the enhancements made in the base implementation by using machine learning techniques. The Gradient model is discussed in detail, along with the methods to include layout effects in the circuit sizing. The concepts and algorithms of all the modules are thoroughly described, enabling readers to reproduce the

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methodologies, improve the quality of their designs, or use them as starting point for a new tool. An extensive set of application examples is included to demonstrate the capabilities and features of the methodologies described.

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